CGO 2004 Program (Proposed --- version 2)

Mon	9-10am		Keynote	"Is Performance Research Done?" Amitabh Srivastava, Microsoft
	10-10:30am		Break	
	10:30-12noon		**Optimizing Memory Performance**	*CJ Newburn, Intel*
		82	Chi-Keung Luk	Ispike: A Post-link Optimizer for the Intel Itanium Architecture
		80	Dongkeun Kim	Physical Experimentation with Prefetching Helper Threads on Intel's Hyper-Threaded Processors
		68	Antonia Zhai	Compiler Optimization of Memory-Resident Value Communication Between Speculative Threads
	12-1:30pm		Lunch	
	1:30-3pm		**New Frameworks**	
		39	Michael Dupre	VHC: Quickly Building an Optimizer for Complex Embedded Architectures
		77	Sungdo Moon	SYZYGY - A Framework for Scalable Cross-Module IPO
		76	Chris Lattner	LLVM: A Compilation Framework for Lifelong Program Analysis & Transformation
	3-3:30pm		Break	
	3:30-5pm		**More Memory Optimizations**	
		6	Kim Hazelwood	Exploring Code Cache Eviction Granularities in Dynamic Optimization Systems
		55	Ali-Reza Adl-Tabatabai	Improving 64-Bit Java IPF Performance by Compressing Heap References
		73	Xiaoming Li	A Memory Hierarchy Conscious and Self-tunable Sorting Library
	5-5:30pm		Break	
	5:30-6:30pm		**Optimizing for Energy Efficiency**	
		40	Ramon Canal	Software-Controlled Operand-Gating
		57	Yoav Almog	Specialized Dynamic Optimizations for High-Performance Energy-Efficient Microarchitecture
			Dinner (on your own)	
Tue	9-10:30am		**Loop Scheduling**	*Stefan Freudenberger, STMicroelectronics*
		70	Mikhail Smelyanskiy	Probabilistic Predicate-Aware Modulo Scheduling
		86	Hongbo Rong	Single-Dimension Software Pipelining for Multi-Dimensional Loops
		90	Hongbo Rong	Code Generation for Single-Dimension Software Pipelining of Multi-Dimensional Loops
	10:30-11am		Break	
	11am-12noon		Keynote	"Evolving the Next Generation of Compilers" Keith Cooper, Rice University
	12-1:30pm		Lunch	
	1:30-3pm		**Instruction Scheduling**	*Jim Dehnert, Transmeta*
		29	Sebastian Winkel	Exploring the Performance Potential of Itanium Processors with ILP-based Scheduling
		54	Manjunath Kudlur	FLASH: Foresighted Latency-Aware Scheduling Heuristic for Processors with Customized Datapaths
		61	Shiliang Hu	Using Dynamic Binary Translation to Fuse Dependent Instructions
	3-3:30pm		Break	
	3:30-5pm		**Code Profiling**	
		31	Youfeng Wu	The Accuracy of Initial Prediction in Two-Phase Dynamic Binary Translators
		32	Rahul Joshi	Targeted Path Profiling: Lower Overhead Path Profiling for Staged Dynamic Optimization Systems
		50	Sriraman Tallam	Extending Path Profiling across Loop Backedges and Procedure Boundaries
	5-6pm		Break	
	6-8pm		Conference dinner	
	9pm		Business meeting	
Wed	9-10am		**Compile-time Optimization**	
		14	Fabrice Rastello	Optimizing Translation Out of SSA Using Renaming Constraints
		45	Yonghua Ding	A Compiler Scheme for Reusing Intermediate Computation Results
	10-10:30am		Break	
	10:30-12noon		**Memory Profiling and Data Layout**	
		91	Byoungro So	Custom Data Layout for Memory Parallelism
		38	Vlad-Mihai Panait	Static Identification of Delinquent Loads
		36	Qiang Wu	Exposing Memory Access Regularities Using Object-Relative Memory Profiling
	12-12:30pm		Closing ceremonies	