Intel® Itanium®
Quad-Core Architecture for the Enterprise

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Agenda

• Introduction
  – Intel® Itanium® Roadmap
  – Intel® Itanium® Processor 9300 Series Overview

• Key Features
  – Pipeline Overview
  – Multithreading
  – Integrated System Interface
  – Performance Monitoring Unit
  – Power and Frequency Management
  – RAS and Manageability

• Questions & Answers
• Multiple product generations on the roadmap
• Powering systems with leading-edge scalability, world-class resiliency, high-end virtualization and intelligent energy efficiency
• Greater choice and flexibility than proprietary RISC solutions
# Tukwila Overview

- **Performance**
  - 4 cores with 2 threads/core
  - High memory and interconnect bandwidth
  - Instruction-level and thread-level parallelism improvements

- **System integration and new system interfaces**
  - Integrated Memory Controllers and Router
  - Intel QuickPath System Interconnect
  - Intel Scalable Memory Interconnect

- **Scalability**
  - Directory coherency with ~2MB of directory cache
  - Up to 8 socket glueless (without a Node Controller chip)
  - Higher scalability with OEM chipsets

- **Power efficiency and performance balance**
  - Dynamic Voltage/Frequency management

- **Reliability, Availability, Serviceability, Manageability**
Die Photo

Dual Integrated Memory Controllers

Quad Multi-Threaded Cores

Power/Thermal/Freq Management

Memory Interface

CrossBar Router

Intel QuickPath Interconnect
Block Diagram

Core 0 + cache
Core 1 + caches
Core 2 + caches
Core 3 + caches

Crossbar Router

Intel® QPI Ports *
4 full-width and 2 half-width Intel QPI links total

Memory Controller
Directory Controller & Cache
Directory Controller & Cache
Memory Controller

Intel® SMI Ports **

Intel® 7500 Scalable Memory Buffer
Intel® 7500 Scalable Memory Buffer
Intel® 7500 Scalable Memory Buffer
Intel® 7500 Scalable Memory Buffer

DDR3 RDIMMs

* Intel® QPI = Intel® QuickPath Interconnect
** Intel® SMI = Intel® Scalable Memory Interconnect
Tukwila Die and Package details

- 65nm bulk CMOS, 8 layer Cu interconnect
- 2.05 billion transistors
- 32.5mm X 21.5mm = 700 mm² die size
- 811 signal package pins in a 1248 pin LGA socket
- 5 major voltage and frequency domains
Execution Cores

- Same high ILP* core as on the 9000/9100 series processor
  - 6 wide instruction fetch, issue & execution
    - 6 integer units, 2 FP units, 4 memory units, 3 branch units
    - 1 cycle L1 data cache
    - Separate L1I, L1D, L2I, and L2D caches
  - Short 8 stage pipeline – high performance and energy efficiency
    - Predication
    - data prefetching and speculation

- Increased core frequency

- Improved memory hierarchy
  - Increased memory bandwidth
  - 4k/8k/16k page size support in first level data TLB

* ILP = Instruction-level parallelism
# Cache Hierarchy

<table>
<thead>
<tr>
<th></th>
<th>L1 Inst Cache per core</th>
<th>L1 Data Cache per core</th>
<th>L2 Inst Cache per core</th>
<th>L2 Data Cache per core</th>
<th>L3 Cache per core</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Size</strong></td>
<td>16 KB</td>
<td>16 KB</td>
<td>512 KB</td>
<td>256 KB</td>
<td>6 MB</td>
</tr>
<tr>
<td><strong>Line Size</strong></td>
<td>64-byte</td>
<td>64-byte</td>
<td>128-byte</td>
<td>128-byte</td>
<td>128-byte</td>
</tr>
<tr>
<td><strong>Ways</strong></td>
<td>4-way</td>
<td>4-way</td>
<td>8-way</td>
<td>8-way</td>
<td>12-way</td>
</tr>
<tr>
<td><strong>Write Policy</strong></td>
<td>-</td>
<td>WT</td>
<td>-</td>
<td>WB</td>
<td>WB</td>
</tr>
<tr>
<td><strong>Latency</strong></td>
<td>1 clk</td>
<td>1 clk</td>
<td>7 clks</td>
<td>5,7,9 clks(^1)</td>
<td>15+ clks(^1)</td>
</tr>
<tr>
<td><strong>Protection</strong></td>
<td>SEC(^2) via Parity</td>
<td>SEC(^2) via Parity</td>
<td>SEC(^2) via Parity</td>
<td>SEC(^2) via ECC</td>
<td>SEC(^2) via ECC</td>
</tr>
</tbody>
</table>

\(^1\) Add 1 clk for FP loads  
\(^2\) SEC: Single Bit Error Correction  

**Note:** Higher level caches do not force inclusion
Switch-on-Event Multithreading

• Switch to alternate thread on specific events
  – Last-level cache demand load miss
  – Data return to last-level cache for inactive thread
  – Explicit thread switch hint instruction
  – Timeout - ensure fairness between threads

• New switch events
  – Semaphore release
  – Extended stalls of execution pipeline
    – Secondary load miss after data prefetch
    – Allows aggressive use of software data prefetching while retaining multithreading benefit

• Thread Switching Controlled by Urgency Logic
  – Tracks relative importance of both threads
  – Switch events modify urgency values
Integrated System Interface

• On-chip Router
  - 12 ports
    – 4 cores, 2 home agents, 4 full-width and 2 half-width external links

• 6 Point-to-point Intel QPI links
  – Higher bandwidth and better scaling than shared buses

• Supports glueless 2 to 8 socket systems
  – One-hop remote memory latency only 40% higher than local memory latency
  – Larger system supported via OEM-provided node controllers

• Directory coherency for efficient scaling
  – Less snoop traffic than broadcast-snoop protocols

• Integrated memory controller
  – Drives external memory buffers to support large memory with high bandwidth
Example Topologies

Glueless systems

... additional cells

Node controller system
Directory Coherency

- **Improved Scalability**
  - Snoop only cache line owners and sharers
  - Snoop traffic is dependent only on workload characteristics
    - Does not scale with the square of system size as in broadcast-snoopy coherency
    - Serial workloads execute with minimal snoop overhead even on large systems

- **Home Agent**
  - Two home agents per processor
  - Receive all requests & issue snoops based on directory state
  - Receive snoop responses & generate final directory and MESI state
  - Data return from home agent or other caches

- **Directory Cache**
  - Caches directory state to reduce snoop latency
  - Snoops overlapped with memory access rather than in series
Integrated Memory Controller

- Memory Controller
  - Associated with home agent
    - Two memory controllers per processor
  - Each drives two Intel Scalable Memory Interface (Intel SMI) channels in lock-step
    - Higher bandwidth and better error correction capability than single channel

- External Memory Buffer
  - Converts point-to-point SMI channel into two independent DDR-3 busses
  - Improved fan-out for greater memory capacity
    - RDIMMs can be located further away from processor for easier board layout and routing
  - Maintains high bandwidth for large memory capacities
    - Electrical load does not slow down high-speed channels
Performance Monitoring Unit

- **Core PMU**
  - Leveraged from previous Itanium designs
    - Pipeline metrics: instruction issue, stalls, thread switches etc.
    - Cache & TLB* metrics: hits, misses, various conflicts
    - Intel QPI Interface: request breakdown, latency
    - Reports CPI** breakdown & memory hierarchy behavior

- **System Interface PMU**
  - Metrics for each major block
    - Router, directory controller, memory controller
    - Transaction breakdown
    - Transaction latency
    - Queuing delay
    - Allows constructing detailed latency breakdown

*TLB = translation look-aside buffer

** CPI = cycles per instruction
Core PMU

- Intel® QPI = Intel® QuickPath Interconnect

Diagram:
- Front End
- Execution Pipeline
- L1I Cache
- L1D Cache
- L2I Cache
- L2D Cache
- L3 Cache
- Memory request latency
- Sampled data reference latency
- Instruction dispersal stalls
- Pipeline stall cycles by type
- Cache pipe stalls
- Cache fills
- Refs / hits / misses by type
- Requests by type
- Snoops by type
- Intel® QPI Interface to Router

* Intel® QPI = Intel® QuickPath Interconnect
System Interface PMU

Crossbar Router

Packets by type

Snoop requests local / remote
Coherency responses by type, originator and destination

Requests by type
Coherency responses by type

Directory Controller and Cache

Request latency including snoops

Memory Controller

Frames by type

Intel® SMI Port **

Intel® QPI Ports *

Snoop latency local / remote

Memory request latency

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** Intel® SMI = Intel® Scalable Memory Interconnect
Dynamic Power Management

• Dynamically adjusts voltage and frequency
  – Maximize performance for a given power and thermal envelope
  – Different applications may run at different frequencies
  – Adjustments are transparent to the OS
  – Digitally estimated power leads to deterministic voltage/frequency changes

• Balances power across all cores
Processor RAS

- All major structures are protected
  - Extensive ECC and parity protection on core and system interface structures and datapaths

- Extensive use of Soft Error hardened (SE-hardened) latches and registers
  - SE-hardened latches/registers are 100x/80x (respectively) less susceptible to soft errors due to alpha particles

- Intel® Cache Safe Technology added to L2I, L2D, and Directory Cache (in addition to L3)
  - Cache lines that show too many errors in the field are mapped out by the processor
Memory RAS Features

- Memory Channel Protection
  - Retry, channel reset & retraining, Intel SMI lane failover

- Patrol and demand scrubbing
  - Prevent uncorrectable errors by writing good data/ECC when encountering a correctable error
    - In background (patrol), or due to a request (demand)

- DRAM Protection – Double Device Data Correction (DDDC)
  - Tukwila can fix both single and double memory hard-errors and still correct an additional single bit error

- Memory channel Hot-Plug Support
  - Replace faulty component without bringing down the system

- Memory Migration and DIMM sparing
System Interconnect RAS

- Intel QuickPath Interconnect protection
  - Retry, reset, retraining
  - Intel QPI lane fail-over

- Hot-Plug Support

- Timeout mechanisms
  - Aids detection of faulty components

- Error Containment mechanisms
  - Error signaling indicates scope of error
Summary

• Improved performance
  – Better thread-level and instruction-level parallelism
  – Higher memory bandwidth

• Improved scalability and platform flexibility
  – Integrated system interface
  – Directory-based coherence protocol

• Power and frequency management capabilities

• Mission Critical RAS: Processor – memory – interconnect

• Launched February 8, 2010

• Multiple OEMs working on Tukwila-based systems

• Performance benchmark results becoming available now
Q&A
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